APPLICATION FOR U.S. PATENT TRANSMITTAL FORM

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10/6/98
J. Dennis Moore, Reg. No. 28,885 Date

Transmitted herewith for filing is the patent application of:

Inventor(s): Gabriel Alfonso Rincon-Mora

For: Active Compensating Capacitive Multiplier
Enclosed are:

13 pages of text and 5 sheets of informal drawings.

An Assignment and Cover Sheet of the invention to TEXAS INSTRUMENTS INCORPORATED.
A Declaration/Power of Attorney of the invention to TEXAS INSTRUMENTS INCORPORATED.

FEE CALCULATION

	NUMBER		NUMBER EXTRA	RATE	FEES
Total Claims	9	- 20 =	0	x $22	$ 000.00
Independent Claims	2	- 3 =	0	x $82	$ 000.00
Basic Fee					**$ 790.00**
			TOTAL FEES		$790.00

Please charge Deposit Account No. 20-0668 in the amount of the Total Fees set forth. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 20-0668. **This form is submitted in triplicate.**

All correspondence related to this application may be addressed to the undersigned at TEXAS INSTRUMENTS INCORPORATED, P.O. Box 655474, MS 3999, Dallas, Texas 75265.

10/6/98
Date

J. Dennis Moore, #28,885
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ACTIVE COMPENSATING CAPACITIVE MULTIPLIER

Technical Field of the Invention

This invention relates to frequency compensation of electronic circuits, and more particularly relates to circuits having compensating capacitors, such as Miller Effect capacitors.

Background of the Invention

The stability performance of circuits having feedback is improved by providing compensation so as to increase phase margin. A well known technique for improving phase margin takes advantage of the Miller Effect, by adding a Miller-compensating capacitance in parallel with a gain stage, e.g., the output stage of a two stage amplifier circuit. Such a configuration results in the well-known and desirable phenomenon called pole splitting, which advantageously multiplies the effective capacitance of the physical capacitor employed in the circuit. See, e.g., for background on compensation of amplifier circuits using Miller-compensating capacitance, Paul R. Gray and Robert G. Meyer, *Analysis and Design of Analog Integrated Circuits*, Third Ed., John Wiley & Sons, Inc., New York, 1993, Ch. 9, especially pp. 607-623.

A problem arises when the load capacitance seen by a circuit having compensating capacitance such as Miller-compensating capacitance becomes large. This requires the compensating capacitance to increase in value in order to maintain stability. However, the larger compensating capacitance occupies more physical space. But, this is not a luxury that can be afforded in an environment where more circuits are integrated onto the same die, which, of course, is the trend.

There is thus a need for a way of dealing with larger load capacitance seen by amplifier circuits having compensating capacitance such as Miller-compensating

capacitance, without placing increasing demands on die area for the circuit. There is also a need to optimize and reduce the silicon area requirement of existing circuit designs using such capacitors, to allow greater chip packing densities, and thus single integrated chip solutions.

Summary of the Invention

The present invention provides an improved compensated amplifier, for amplifying an input signal applied to an input node to provide an output signal at an amplifier output node. The compensated amplifier includes a first amplifier stage having an internal node functioning as an input thereto and having a first stage output node. Also included is a second amplifier stage coupled to the first amplifier stage, having the input node as an input thereto and providing the output signal at the amplifier output node. A capacitor is coupled between the output node and the internal node.

The invention may be advantageously applied for the purpose of multiplying Miller-compensating capacitance, although it is not limited to that application.

It is to be understood that the term "amplifier" as used herein is not limited to any specific form of amplifier, such as an operational amplifier. Rather, the term is intended to refer to any circuit that provides an amplified form of an input signal applied thereto.

These and other features of the invention will be apparent to those skilled in the art from the following detailed description of the invention, taken together with the accompanying drawings.

Brief Description of the Drawings

Fig. **1** is a schematic diagram of a prior art differential amplifier including a Miller-compensating capacitor.

Fig. **2** is a schematic diagram of a differential amplifier including a Miller-compensating capacitor provided in accordance with the principles of the present invention.

Fig. **3** is a diagram showing an ac-equivalent circuit model of the amplifier circuit of Figure **2**.

Fig. **4** is a schematic diagram of a simple amplifier including a compensating capacitor provided in accordance with the principles of the present invention.

Fig. **5** is a diagram showing an ac-equivalent circuit model of the amplifier circuit of Figure **4**.

Detailed Description of the Preferred Embodiment

Figure **1** is a schematic diagram of a prior art differential amplifier **10** including a Miller-compensating capacitor **C1**. A supply voltage V_{DD} is provided between a supply rail **12** and a ground rail **13**. A sinking bias current i_B is provided on an input line **14**. A differential input is provided, with the positive going signal V_p being provided on input line **16** and the negative going signal V_n being provided on input line **18**. The amplifier **10** structure is two stage. The first stage **20** is a folded-cascode differential amplifier. The second stage **22** is a Miller-compensated PMOS device amplifier.

In the first stage **20**, the differential inputs on lines **16** and **18** are provided to the respective gates of a pair of PMOS devices **24**, **26**. The differential current generated through devices **24**, **26**, is reflected into NMOS devices **28**, **30**. The voltage on the drain of device **30** is sensed at the gate of output PMOS device **32**. Capacitor **C1** and resistor **R1**, series connected between the drain and gate of device **32**, provide Miller compensation for amplifier **10**.

The other circuitry of amplifier **10** is provided for the various biases required by amplifier **10**. Thus, NMOS device **34** provides a quiescent bias current for output PMOS transistor **32**. PMOS device structure **38** is a multiple output current mirror. Device **40** is diode-connected and establishes a stable internal bias voltage, based on the input bias current i_B on line **14**. This stable bias current i_B is thus mirrored by devices **42**, **44**, **46**, and **48**. The mirrored current in device **42** is converted into another stable bias voltage by NMOS device **50** at node **52**, which biases the gates of devices **28**, **30**. The mirrored current in device **44** is also mirrored by NMOS current mirror **54** to force current generation via node **56** through device **28** and device **24**. Likewise, the mirrored current in device **48** is also mirrored by NMOS current mirror **58** to force current generation via node **60** through device **30** and device **26**. The mirrored current in device **46** provides a stable bias current for devices **24** and **26**.

Finally, the current mirror **64** provides an ac path and a stable current supply, via lines **66** and **68**, to devices **28** and **30**, respectively.

The circuit **10** described above in Figure **1** is known, and provides good performance. In fact, the use of a Miller-compensating capacitor results in a multiplication of the effective compensating capacitance, enhancing the desirable, and known, effect of pole splitting. However, as the load capacitance on output node **36** increases, the Miller-compensating capacitor **C1** must also increase in value to maintain stability in the circuit **10**. This can result in capacitor **C1** occupying more physical space than is desired, or even than can be afforded.

Figure **2** is a schematic diagram of a differential amplifier **100** including a Miller-compensating capacitor **C2** provided in accordance with the principles of the present invention. Similar to the circuit **10** of Figure **1**, the amplifier **100** structure is two stage, the first stage **20'** being a folded-cascode differential amplifier, and the second stage **22'** being a Miller-compensated PMOS device amplifier. Unlike the circuit **10** of Figure **1**, however, Miller-compensating capacitor **C1** and resistor **R1** are not provided.

Instead, the circuit **100** of Figure **2** includes a novel capacitor arrangement consisting of capacitor **C2** connected between the output node **36'** and the common connection node **102** for the gates of the two NMOS devices–an NMOS device **104** diode-connected, and an NMOS device **106** ratioed by a factor of ten as compared with device **104**, comprising current mirror **54'**. By connecting capacitor **C2** in this way, the feedback current flowing through capacitor **C2** is amplified, i.e. multiplied by, e.g., ten by current mirror **54'** before reaching the high impedance node **68**. The resulting load capacitance seen by the high-impedance node **68** is then ten times greater than the Miller-multiplied version connected using prior art principles. Thus, there is provided by the present invention a multiplication of an effective capacitance that is itself a multiplied, effective capacitance.

Note that the value ten for the multiplication factor described above is arbitrary, and is selected for example only. The gain, and thus the multiplication

factor, is ultimately achieved in the circuit of Figure **2** by the effective current amplification by current mirror **54'**, and its limitation depends on the physical restrictions, or spread, of current mirror **54'**. In the circuit of Figure **2** the mirror ratio of the current flowing through current mirror **54'**, i.e., the ratio of the widths of device **106** and device **104**, and thus the ratio of the current flowing through device **106** as compared with device **104**, is ten. Other ratios, and thus other capacitance multiplication factors are possible. The width of PMOS device **44** is reduced by the same ratio. For optimal matching performance (low input offset), PMOS device **48** and current mirror **58** are made to match PMOS device **44** and current mirror **54**. Key is the amplification of the compensating capacitor's current.

Figure **3** shows an ac-equivalent model **200** of the amplifier circuit of Figure **2**. The model **200** has two stages, a first stage **210** and a second stage **220**. As shown, in first stage **210** a differential input voltage $\mathbf{V_{in}}$ ($\mathbf{V_{in}} = \mathbf{V_p} - \mathbf{V_n}$) produces a current of $\mathbf{g_{m1}V_{in}}$ in equivalent transconductor **212**. In the second stage **220**, a voltage $\mathbf{V_x}$ is seen at the input of Miller-compensating capacitance $\mathbf{C_m}$ and an ac current $\mathbf{I_x}$ flows through internal resistance $\mathbf{R_i}$. The current $\mathbf{I_x}$ is reflected back through block **214**, multiplied by ten, to the input circuit **210**.

The transfer function of the circuit model **200** of Figure **3** may be derived as follows:

Eq. 1 $$I_x = (V_o - V_x)C_m s$$

Eq. 2 $$V_x = \frac{V_o R_i C_m s}{1 + R_i C_m s}$$

Eq.3 $$V_o = -\{[V_{in} g_{m1} + 10\, I_x] r g_{m2} + I_x\} R_o$$

Combining Equations 1, 2 and 3 yields:

Eq. 4 $$\frac{V_o}{V_i} \cong \frac{-(g_{m1} r g_{m2} R_o)(1 + R_i C_m s)}{1 + C_m s(R_i + 10 r g_{m2} R_o)} \approx \frac{-g_{m1} r g_{m2} R_o (1 + R_i C_m s)}{1 + C_m s 10 r g_{m2} R_o}$$

Note in Equation 4 that there is no right-hand plane zero. In fact, a Left Hand Plane (LHP) zero is inserted. This LHP zero can be used to optimize the compensation of the loop in Figure **2** created by the connection of capacitor **C2** between the output node **36'** in the second stage **22'** and the common gate connection of devices **104** and **106** in the first stage **20'**, which is controlled by the transconductance of device **104**. The dominant pole for the circuit **100** of Figure **2** is defined by the high impedance node **68** and ten times the gain of the second stage **22'** times the Miller-compensating capacitance **C2**. For instance, the LHP zero can be designed to lie approximately where the pole of output node **36'** lies. As a result, the pole is cancelled and phase margin is consequently increased.

Figure **4** is a graph showing Bode plots of the behavior of different circuits like the circuit shown in Figure **1** and the circuit shown in Figure **2**. This figure helps in understanding the principles presented in the immediately preceding paragraph. Two different sets of curves **236, 238**, are shown in Figure **4**. As can be seen, while there is one horizontal axis **230**, representing frequency and divided into units of Hertz, there are two vertical axes, a first axis **232**, representing the gain of the respective circuit and divided into units of decibels ("DB"), and a second axis **234**, representing the relative phase of the output signal as compared with the phase of the input signal, and divided into units of degrees. The first set of curves **236** is plotted against the gain axis **232**, while the second set of curves **238** is plotted against the phase shift axis **234**. In the set of curves **238** a zero relative phase compared with the input is 0°, which is the same as 360°. In all of the circuits represented in Figure **4**, as frequency increases the phase of the output signal tends to lag more, as compared with the phase of the input signal, and thus it will be noted that the curves **238** all tend to drop, showing a decrease in phase from 360° as frequency increases. In addition, in all of the circuits represented in Figure **4**, as frequency increases the gain tends to drop, and thus it will be noted that the curves **236** all tend to drop, showing a decrease in gain as frequency increases.

A first curve **240** is a plot of the gain of a representative circuit constructed like that of Figure **1**, against frequency, in which the compensating-capacitance **C1** is 2 pF. A second curve **242** is a plot of the relative phase of the output signal V_o as compared with the phase of the input signal $V_{in} = V_p - V_n$ for the same circuit. Note that at the frequency at which the unity gain point **244** exists for curve **240** the relative phase, shown by point **246**, is approximately 140°, which represents a phase shift of –220°, or 40° more than the –180° limit for stable operation.

A third curve **248** is a plot of the gain of a representative circuit constructed like that of Figure **1**, against frequency, in which the compensating-capacitance **C1** is 20 pF. A fourth curve **250** is a plot of the relative phase of the output signal V_o as compared with the phase of the input signal V_{in} for the same circuit. Note that at the frequency at which the unity gain point **252** exists for curve **248** the relative phase, shown by point **254**, is approximately 200°, which is a phase shift of only –160°, which is within the –180° limit for stable operation.

Now, a fifth curve **256** is a plot of the gain of a representative circuit constructed like that of Figure **2**, against frequency, in which the compensating-capacitance **C2** is 2 pF. A sixth curve **258** is a plot of the relative phase of the output signal V_o as compared with the phase of the input signal V_{in} for the same circuit. Note that at the frequency at which the unity gain point **260** exists for curve **256** the relative phase, coincidentally also shown by point **260**, is approximately 270°, which is a phase shift of only –90°, which is well within the –180° limit for stable operation. In fact, stable operation continues well beyond the unity gain frequency. Thus, the extension of curve **258** in the manner shown so as to increase the phase margin shows how the LHP zero can be placed strategically so as to enhance the stability of the circuit of Figure **2**.

The technique may also be extended to simple compensated amplifiers that do not have Miller-compensating capacitance. Figure **5** illustrates one such implementation. In this instance, the technique is used to effectively multiply the

compensating capacitor **C**. NMOS device **MN2** is ten times larger than NMOS device **MN1**, providing a multiplication factor of eleven; current I_x is sensed by **MN1** and multiplied by ten by **MN2**. Thus, the effective capacitive current is $I_x + 10I_x$, hence the multiplication factor of eleven, again a factor chosen arbitrarily. A LHP zero is also inserted in this embodiment. The resulting transfer function, illustrated by the ac-equivalent circuit model shown in Figure **6**, is roughly:

Eq. 5
$$\frac{V_{out}}{V_{in}} \approx \frac{-g_{mp1}\left(r_{\delta s-MP1} // r_{\delta s-MN2}\right)\left(1+\frac{Cs}{g_{MN2-MN1}}\right)}{1+s(11C)\left(r_{\delta s} // r_{\delta s-MN1}\right)}$$

where Equations 1 and 2 still apply. Note that in Figure **6**

$$r_{\delta S} = r_{\delta sMN2} // r_{\delta sMP1}.$$

Finally, note that while the circuits disclosed herein are all made of MOS devices, the principles are applicable as well to circuits made of bipolar devices. For example, a bipolar current mirror could be used as a current amplifier in much the same way as the NMOS current mirror **54'** of Figure **2**, to provide the effective multiplication of capacitance.

Although the present invention and its advantages have been described in detail, as well as some variations over the disclosed embodiments, it should be understood that various other changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

What is Claimed is:

1. A compensated amplifier, for amplifying an input signal applied to an input node to provide an output signal at an amplifier output node, comprising:

a first amplifier stage having an internal node as an input thereto and having a first stage output node;

a second amplifier stage coupled to said first amplifier stage, having said input node as an input thereto and providing said output signal at said amplifier output node; and

a capacitor coupled between said output node and said internal node.

2. A compensated amplifier according to Claim 1, wherein said second amplifier stage is coupled to said first amplifier stage such that said first stage output node is common with said amplifier output node.

3. A compensated amplifier according to Claim 1, wherein said second amplifier stage is coupled to said first amplifier stage such that said first stage output node is connected to said input node.

4. A compensated amplifier according to Claim 1, wherein said capacitor is connected such that a left-hand-plane zero is provided in said compensated amplifier.

5. A compensated amplifier according to Claim 4, wherein said left-hand-plane zero is selected so as to optimize compensation for said compensated amplifier.

6. A compensated amplifier according to Claim 1, wherein said first amplifier stage comprises a bipolar transistor current mirror.

7. A compensated amplifier according to Claim 1, wherein, in operation, capacitive current flows through said capacitor, and said capacitive current is sensed at said internal node and amplified by said first amplifier stage.

8. A compensated amplifier according to Claim 7, wherein said first amplifier stage comprises a diode connected transistor and a ratioed transistor connected together forming a current mirror, and wherein said diode connected transistor senses said capacitive current at said internal node and said ratioed transistor amplifies said capacitive current.

9. A Miller-compensated amplifier, for amplifying an input signal applied to an amplifier input node to provide an output signal at an amplifier output node, comprising:

a first amplifier stage having an internal node as an input thereto, and having a first stage output node;

a second amplifier stage having said amplifier input node as an input thereto, and having a second stage output node;

a third amplifier stage having a third stage input node coupled to said first stage output node and to said second stage output node, and providing said output signal at said amplifier output node; and

a capacitor coupled between said amplifier output node and said internal node.

Abstract of the Disclosure

A compensated amplifier, for amplifying an input signal applied to an input node to provide an output signal at an amplifier output node. The compensated amplifier includes a first amplifier stage having an internal node as an input thereto and having a first stage output node. Also included is a second amplifier stage coupled to the first amplifier stage, having the input node as an input thereto and providing the output signal at the amplifier output node. A capacitor is coupled between the output node and the internal node.

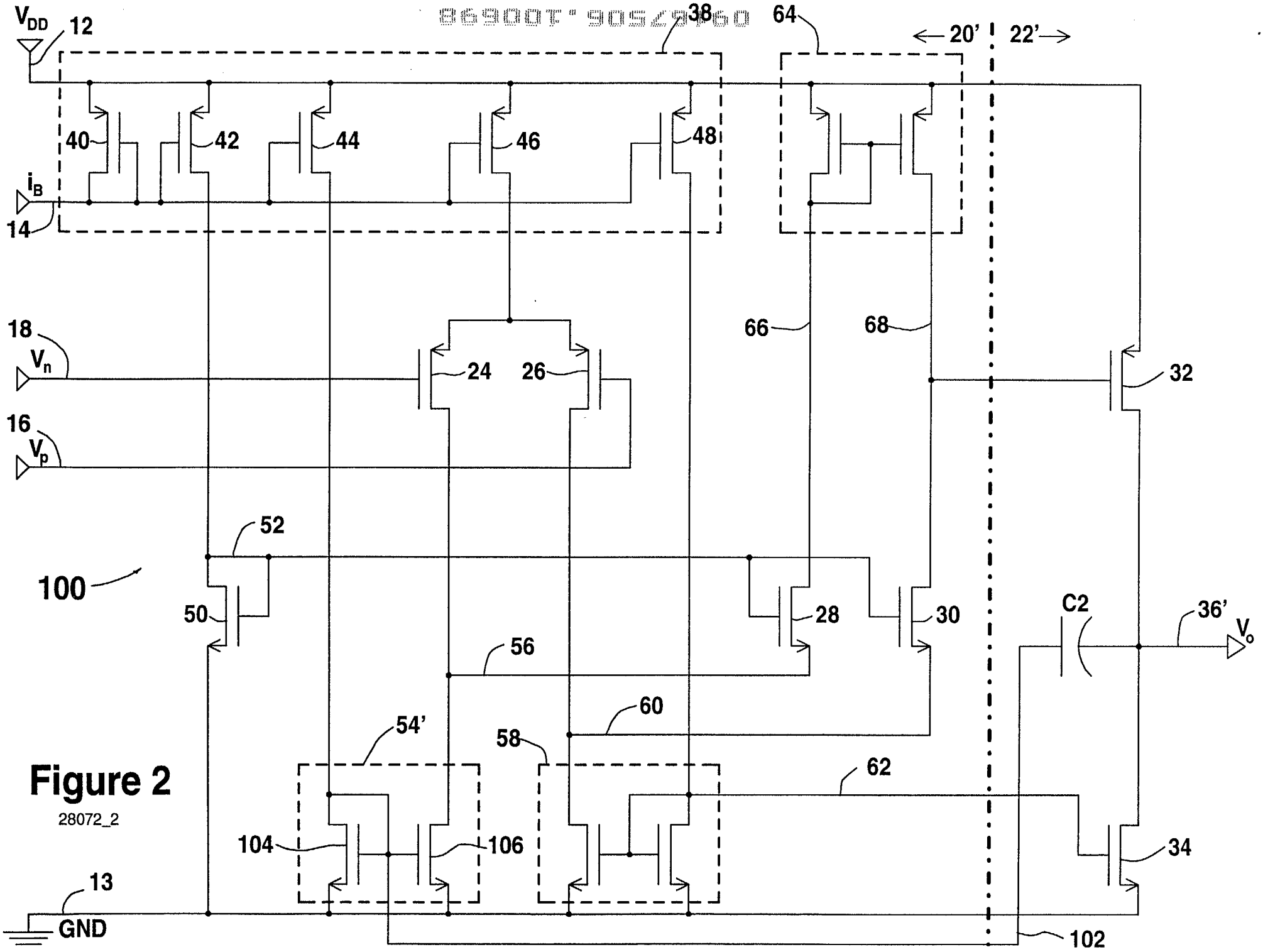

Figure 2

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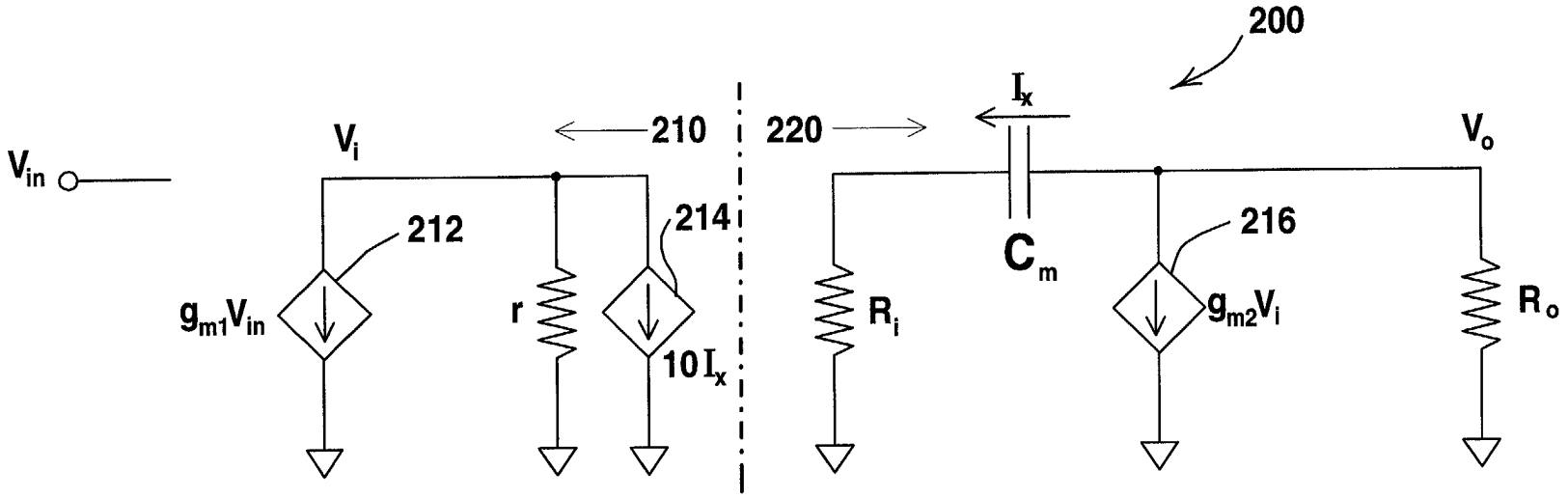

Figure 3

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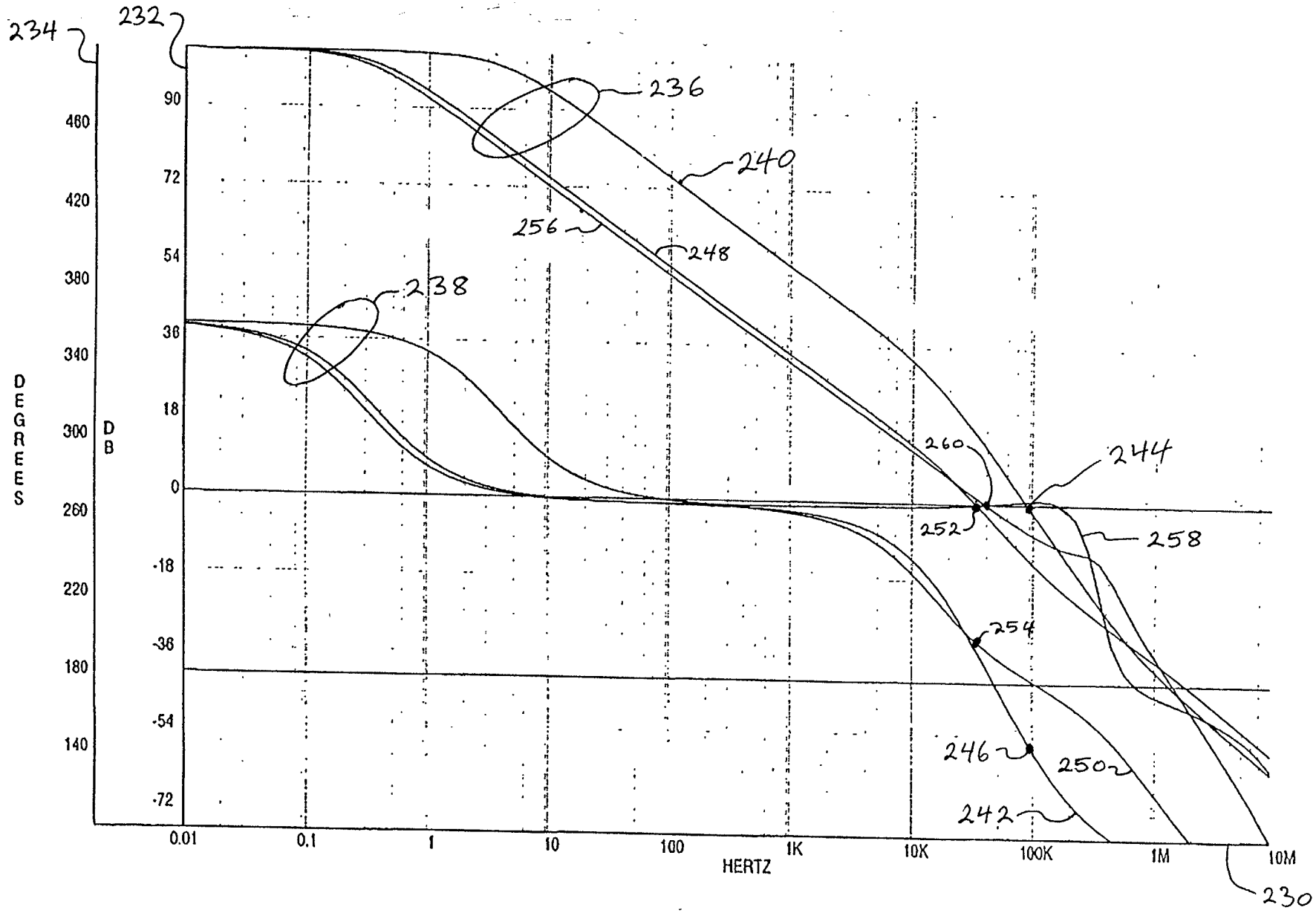

Figure 4

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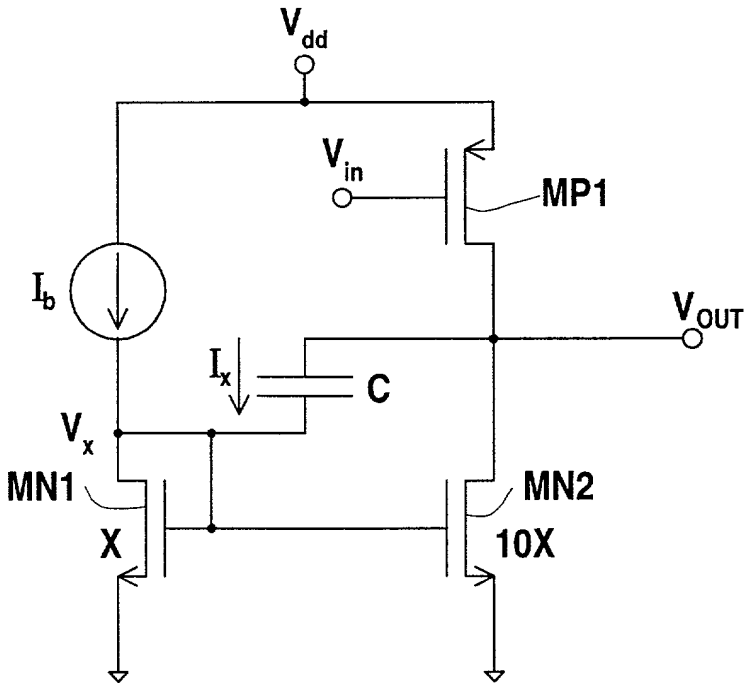

Figure 5

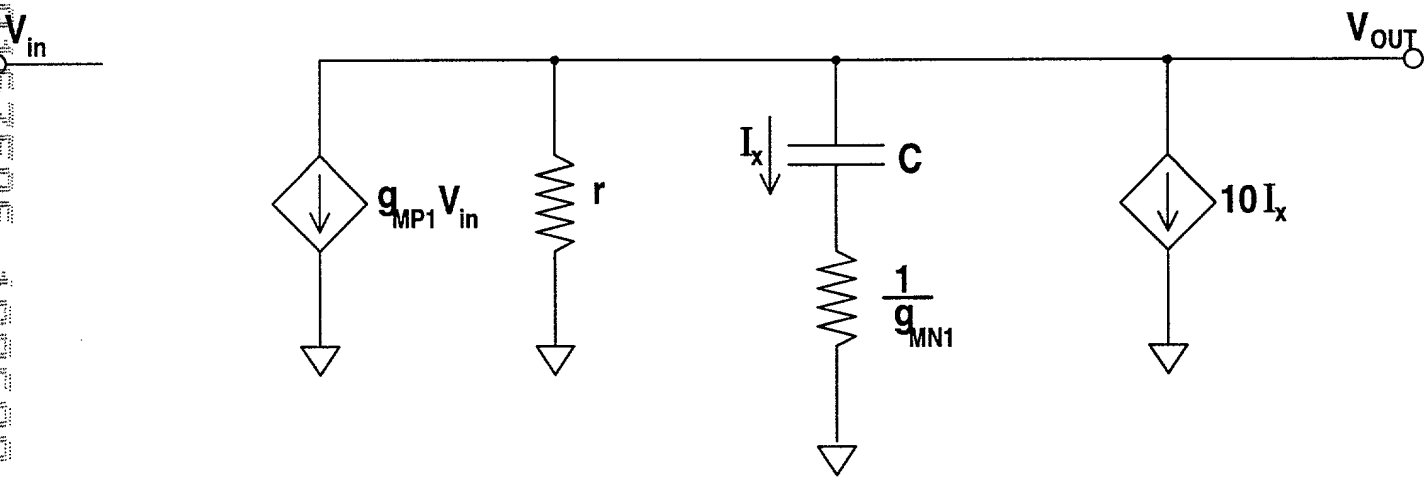

Figure 6

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ATTORNEY'S DOCKET NO
TI-28072

APPLICATION FOR UNITED STATES PATENT
DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I declare that my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor if only one name is listed below, or an original, first and joint inventor if plural inventors are named below, of the subject matter which is claimed and for which a patent is sought on the invention entitled as set forth below, which is described in the attached specification; that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in the oath or declaration; that no application for patent or inventor's certificate on this invention has been filed by me or my legal representatives or assigns in any country foreign to the United States of America; and that I acknowledge my duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56;

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

TITLE OF INVENTION:

Active Compensating Capacitive Multiplier

POWER OF ATTORNEY: I HEREBY APPOINT THE FOLLOWING ATTORNEYS TO PROSECUTE THIS APPLICATION AND TRANSACT ALL BUSINESS IN THE PATENT AND TRADEMARK OFFICE CONNECTED THEREWITH

Richard L. Donaldson, #25,673; Jay M. Cantor, #19,906; William B. Kempler, #28,228 and J. Dennis Moore, #28,885

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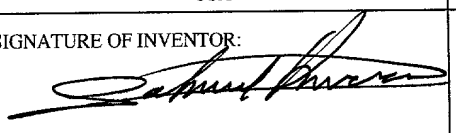
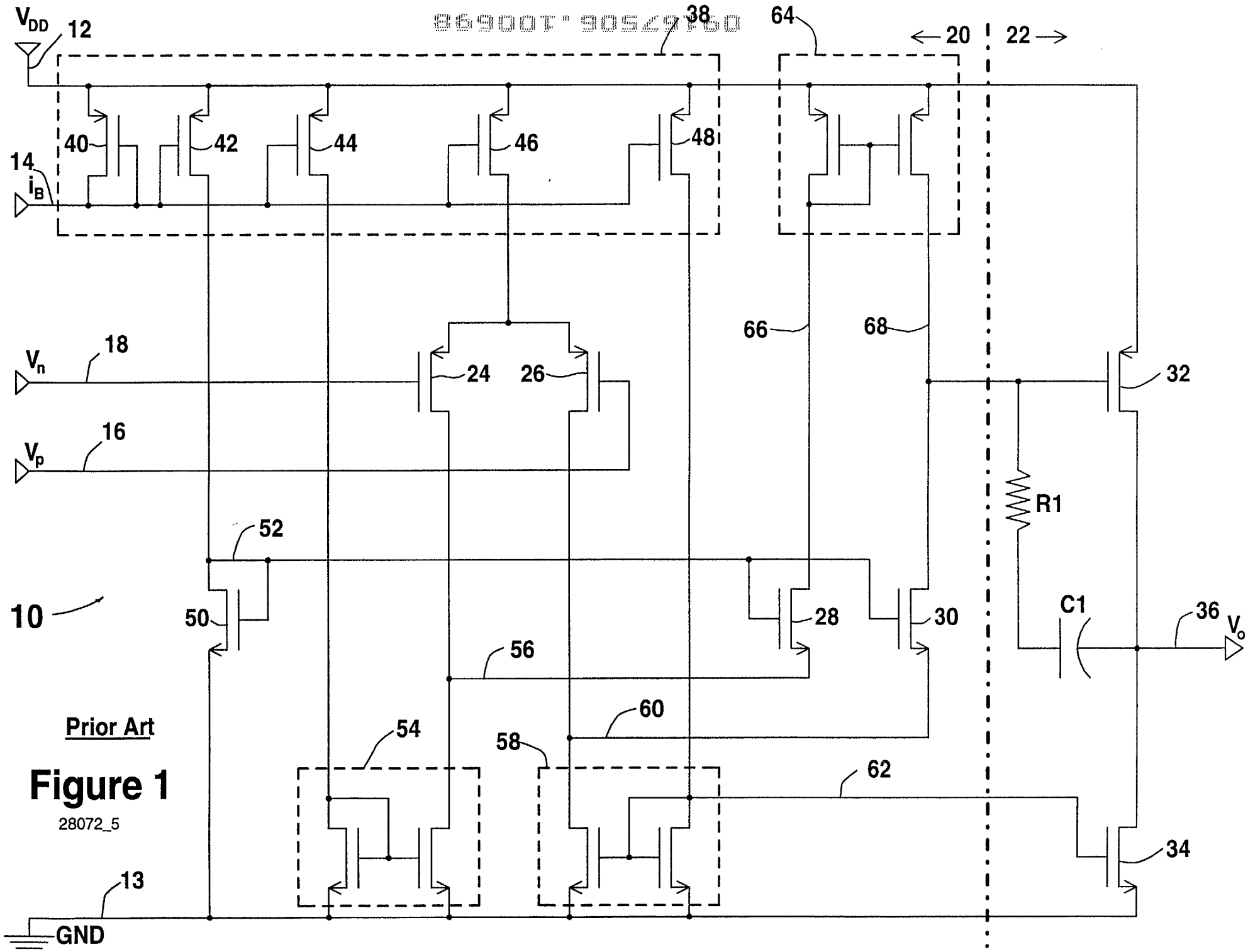
COUNTRY OF CITIZENSHIP: USA	COUNTRY OF CITIZENSHIP:	COUNTRY OF CITIZENSHIP:
SIGNATURE OF INVENTOR: X 	SIGNATURE OF INVENTOR:	SIGNATURE OF INVENTOR:
DATE: X 10-5-98	DATE:	DATE:



Prior Art

Figure 1

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